Multi-Level Nanoimprint Lithography for TFT Display Manufacturing

Auke Jisk Kronemeijer[1], Lukasz Witczak[1], Tamer Dogan[2], Joris de Riet[1], Thijs Bel[1], Roy Verbeek[1], Joris Maas[1] , Ilias Katsouras[1] and Gerwin Gelinck[1,2]

[1] TNO / Holst Centre High Tech Campus 31, NL-5656 AE
Eindhoven, The Netherlands
[2] Dept. Department of Applied Physics, Eindhoven University of Technology
5600MB, Eindhoven, The Netherlands

E-mail: auke.kronemeijer@tno.nl

The display industry continues to push to higher resolution displays as well as lower manufacturing costs. Nanoimprint lithography (NIL) promises both. It can offer high-pattern fidelity over large area at low cost [1,2]. Multi-level imprinting can be used to fabricate thin-film transistors.

Using single-layer NIL, we demonstrate the realization of functional short-channel top-gate a-IGZO thin-film transistors (TFTs) with channel lengths down to 450 nm using nanoimprint lithography. TFTs with a field-effect mobility 10 cm2·V−1·s−1, subthreshold swing (SS) of 0.3 V/decade, and a near-zero turn-on voltage, were obtained after process optimization [3].

Using multi-level NIL promises further simplification of the TFT fabrication. By ‘encoding’ the information of multiple, critical layers of the TFT in a single imprint step, we can further reduce the number of mask steps, and secure overlay accuracy between critical layers at the same time [4,5]. We demonstrate a-IGZO TFTs using a multi-level nanoimprint lithography approach. We believe our results provide an incentive for further exploration of NIL for cost-effective realization of (sub-μm channel) a-IGZO TFTs.

This work is financed through the Flexlines project within the Interreg V-programme Flanders-The Netherlands, a cross-border cooperation programme with financial support from the European Regional Development Fund, and co-financed by the Province of Noord-Brabant, The Netherlands.

References:

[1] L. J. Guo, Adv. Mater. 19, 495 (2007).
[2] P. J. Renstrom et al. J. Vac. Sci. Technol. B, 14, 4129 (1996)
[3] S. Ram et al., IEEE Trans. Electron. Devices 66, 1778 (2019). A.J. Kronemeijer et al. IEEE Trans. Electron. Devices 66, 1778 (2019).
[4] H.J. Kim et al. J. SID 17/11, 963 (2009).
[5] W.B. Jackson, Chapter 5 in ‘Flexible Electronics: Materials and Applications’ eds. W.S. Wong, A. Salleo. Springer Science, DOI 10.1007/978-0-387-74363-9 5.

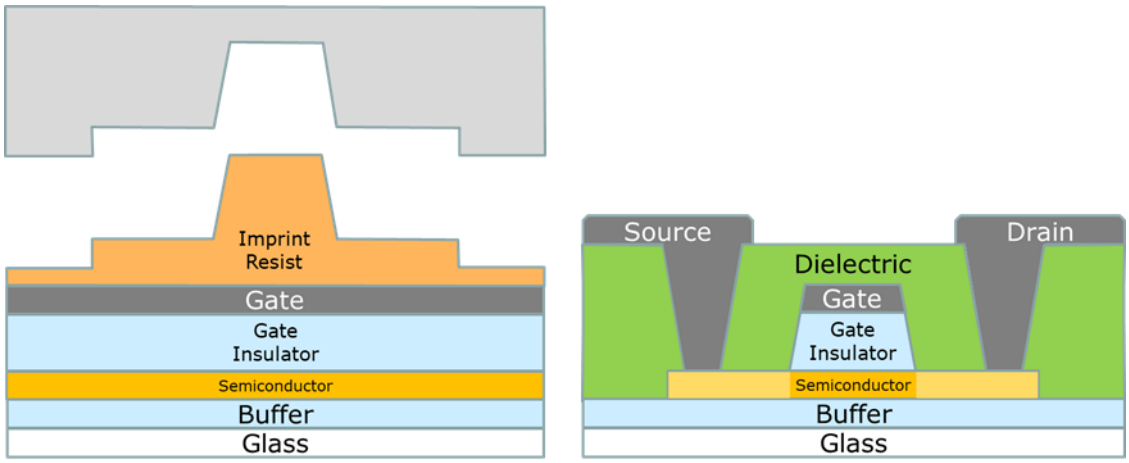

Fig. 1. Schematic of the multi-level imprint lithography concept for the realization of top-gate a-IGZO thin-film transistors (TFTs).

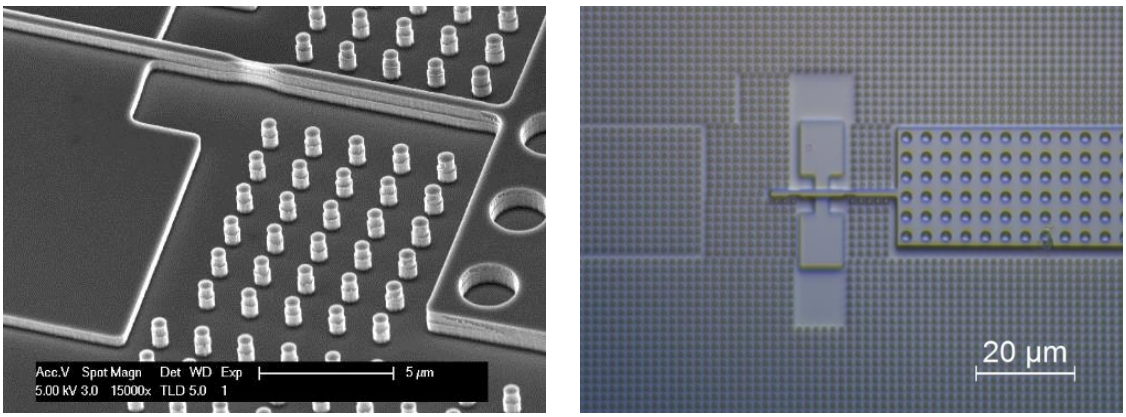

Fig 2. SEM image of the multi-level top-gate a-IGZO TFT imprint master, and microscope image of reproduced multi-level TFT resist pattern.