Design for nanoimprint lithography:
Hot spot modification
through total NIL process simulation

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Nano-imprint lithography (NIL) has been developed targeting various devices, and for its pattern fidelity toward the fabrication of fine pattern without using multiple patterning (Figure 1)[1-3] steps, extensions into fine pattern devices such as semiconductor memories have been expected. Layout and process dependent hotspots extraction and modification has become a significant issue for high volume manufacturing (HVM) of devices with smaller pattern size and, design for manufacturing (DFM) flow utilizing NIL process simulation incorporating a model of the nano-imprint process has become necessary.

Process simulation models those are utilized in NIL have been summarized in Figure 2 (a). In the case of Jet and Flash Imprint Lithography (J-FIL), in which resist drops are dispensed using ink-jet method, major NIL process steps are, resist drop placement through inkjet nozzle, template imprinting, UV curing and de-molding. NIL process simulations corresponding to each steps are needed. Dominant resist related factors and corresponding size scale is summarized in Figure 2 (b). The major issue is that the resist flow behavior in the nanometer scale, which is still very unclear, must be considered in the simulation of NIL. In the smaller sized space under 15 nm, resist viscosity has been observed to be increased. To elucidate the mechanism, detailed measurement of resist behavior and characteristics in the finer space is necessary[4-5]. An example of pattern collapse analysis using resist fluid simulation is illustrated in Figure 3.

In this paper, various NIL process simulation[6-8] methods, system flow, comparison of simulation and experimental data, issues and development prospects are elaborated.

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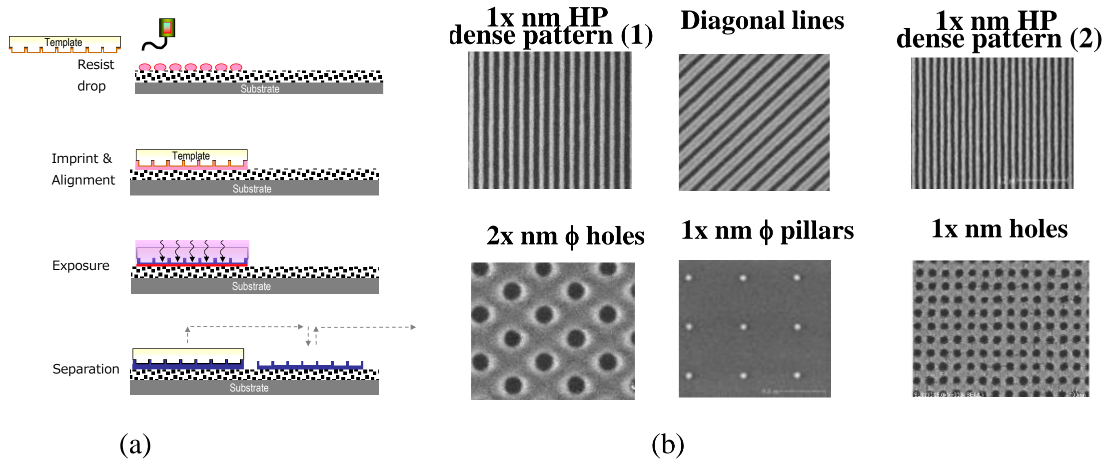
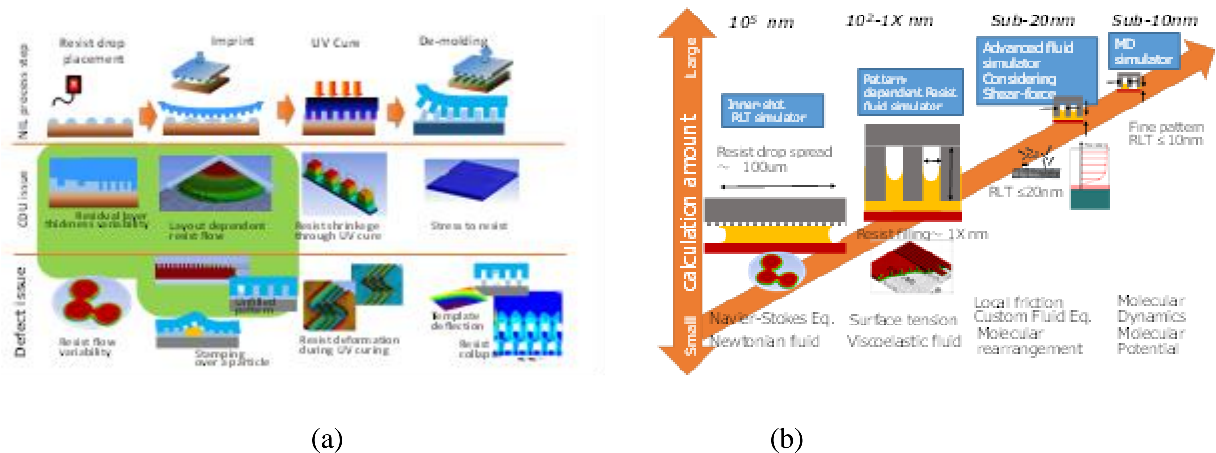


(a) (b)

Figure 1. (a) Jet and Flash Imprint Lithography process, (b) Examples of experimental result patterned by NIL.



(a) (b)

Figure 2. (a) Simulation model utilized in NIL. (b) Physical modes for resist behavior depending on the size.

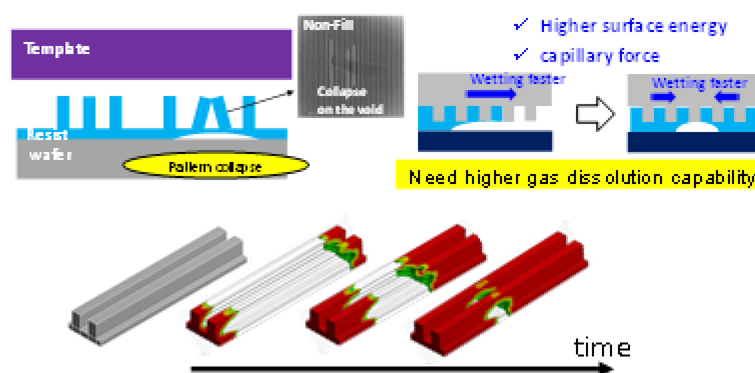


Figure 3. Pattern collapse occurs partially caused by bubble trap on the substrate. The resist flow behavior is shown using resin fluid simulator.